WHAT IS CLAIMED IS:

1. A multi-channel serdes receiver, comprising:

a central frequency synthesizer; and

a plurality of channel-specific receivers coupled to said central frequency synthesizer, each of said plurality including a clock recovery circuit having a phase detector and a phase interpolator, said clock recovery circuit coupling said phase detector and said central frequency synthesizer.

2. The receiver as recited in Claim 1 wherein said central frequency synthesizer includes a voltage-controlled oscillator.

3. The receiver as recited in Claim 1 wherein said central frequency synthesizer is a phase-locked loop.

4. The receiver as recited in Claim 1 wherein said plurality further includes at least one integrator coupled to said phase interpolator and a demultiplexer.

5. The receiver as recited in Claim 4 wherein said at least one integrator performs an integrate-and-dump function.

6. The receiver as recited in Claim 1 wherein said clock

recovery circuit comprises a delay-locked loop clock and data recovery circuit.

7. The receiver as recited in Claim 1 wherein said central frequency synthesizer provides both in-phase and quadrature-phase clock signals.

8. The receiver as recited in Claim 1 wherein said plurality includes two integrators configured to perform a first 1:2 demultiplexing operation.

9.The receiver as recited in Claim 8 further comprising four latches coupled to said integrators and configured to perform a second 1:2 demultiplexing operation.

10. The receiver as recited in Claim 1 further comprising a clock generation circuit coupled to said phase interpolator and configured to generate a plurality of clock signals.

11. The receiver as recited in Claim 10 further comprising at least one synchronizer configured to reduce skew between said plurality of clock signals.

12. A method of operating a multi-channel serdes receiver, comprising:

generating a central clock signal with a central frequency synthesizer; and

transmitting said central clock signal to a plurality of channel-specific receivers coupled to said central frequency synthesizer, each of said plurality including a clock recovery circuit having a phase detector and a phase interpolator, said clock recovery circuit coupling said phase detector and said central frequency synthesizer.

13. The method as recited in Claim 12 wherein said central frequency synthesizer includes a voltage-controlled oscillator.

14. The method as recited in Claim 12 wherein said central frequency synthesizer is a phase-locked loop.

15. The method as recited in Claim 12 wherein said plurality further includes at least one integrator coupled to said phase interpolator and a demultiplexer.

16. The method as recited in Claim 15 wherein said at least one integrator performs an integrate-and-dump function.

17. The method as recited in Claim 12 wherein said clock recovery circuit comprises a delay-locked loop clock and data recovery circuit.

18. The method as recited in Claim 12 wherein said central clock signal contains both in-phase and quadrature-phase clock signals.

19. The method as recited in Claim 12 wherein said plurality includes two integrators, said integrators performing a first 1:2 demultiplexing operation.

20. The method as recited in Claim 12 further comprising four latches coupled to said integrators, said latches performing a second 1:2 demultiplexing operation.

21. The method as recited in Claim 12 further comprising a clock generation circuit, coupled to said phase interpolator, generating a plurality of clock signals.

22. The receiver as recited in Claim 21 further comprising reducing a skew between said plurality of clock signals with at least one synchronizer.

23. An integrated circuit, comprising:

a substrate; and

a plurality of circuit layers located over said substrate and arranged to form a multi-channel serdes receiver that includes:

a central frequency synthesizer, and

a plurality of channel-specific receivers coupled to said central frequency synthesizer, each of said plurality including a clock recovery circuit having a phase detector and a phase interpolator, said clock recovery circuit coupling said phase detector and said central frequency synthesizer.

24. The integrated circuit as recited in Claim 23 wherein said central frequency synthesizer includes a voltage-controlled oscillator.

25. The integrated circuit as recited in Claim 23 wherein said central frequency synthesizer is a phase-locked loop.

26. The integrated circuit as recited in Claim 23 wherein said plurality further includes at least one integrator coupled to said phase interpolator and a demultiplexer.

27. The integrated circuit as recited in Claim 26 wherein said at least one integrator performs an integrate-and-dump function.

28. The integrated circuit as recited in Claim 23 wherein said clock recovery circuit comprises a delay-locked loop clock and data recovery circuit.

29. The integrated circuit as recited in Claim 23 wherein said central frequency synthesizer provides both in-phase and quadrature-phase clock signals.

30. The integrated circuit as recited in Claim 23 wherein said plurality includes two integrators configured to perform a first 1:2 demultiplexing operation.

31. The integrated circuit as recited in Claim 23 further comprising four latches coupled to said integrators and configured to perform a second 1:2 demultiplexing operation.

32. The integrated circuit as recited in Claim 23 further comprising a clock generation circuit coupled to said phase interpolator and configured to generate a plurality of clock signals.

33. The integrated circuit as recited in Claim 32 further comprising at least one synchronizer configured to reduce skew between said plurality of clock signals.

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